

PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Wadgi W. Abadeer, et al.

Examiner: Vinh P. Nguyen

Serial N : 09/811,915

Art Unit: 2829

Filed: March 19, 2001

Docket: BUR920000082US1 (13647)

For: A WAFER LEVEL SYSTEM FOR  
PRODUCING BURN-IN/SCREEN,  
AND RELIABILITY EVALUATIONS  
TO BE PERFORMED ON ALL CHIPS  
SIMULTANEOUSLY WITHOUT ANY  
WAFER CONTACTING

Dated: February 25, 2003

Assistant Commissioner for Patents  
Washington, D.C. 20231

AMENDMENT UNDER 37 C.F.R. 1.111

Sir:

In response to the Office Action of November 25, 2002, applicants respectfully  
request that the following amendments be entered into this application:

IN THE CLAIMS:

Please amend Claims 1, 2, 4, 5, 10, 11, 26, 27, 30, 35 and 36 as follows

1. (Amended) A method for electrically stressing through a specified voltage at least one  
semiconductor chip on a wafer for controlled contactless burn-in, voltage screen and

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal  
Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents,  
Washington, D.C. 20231, on February 25, 2003.

Dated: February 25, 2003Mishelle Mustafa

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